Electronic Photonic Integrated Circuits for Data Center Interconnects

G. Mehrpoor[1,2], B. Wohlfeil[1], M. Eiselt[1], J.P. Elbers[1], B. Schmauss[2]

[1]ADVA Optical Networking SE, 98617 Meiningen, Germany
[2]LHFT, Friedrich-Alexander Universität Erlangen-Nürnberg, 91058 Erlangen, Germany
gmehrpoor@advaoptical.com

Data center interconnects (DCI) are reaching a demanding point for the establishment of connections between the data centers in metro and long-haul networks. The current optical transceivers, building blocks of the DCIs, operate at 100 Gb/s, however, the increasing need for bandwidth, small footprint and cost efficiency demands an upgrade of this rate to 400 Gb/s. Subsequently, it causes converging of new technologies at different levels of the transceiver assembly to find enabling solutions for the traffic growth in next generation cloud based applications and interconnection.

Silicon is a solution platform for a higher-level integration of electronics and photonics. Two typical technology approaches are available for this purpose. In hybrid integration, electronic and photonic chips are fabricated independently and combined afterwards [1]. Whereas, monolithic integration on a single chip decreases the total dimensions, enabling shorter electrical trace lengths and improved RF performance. Photonic BiCMOS technology is a promising candidate for this type of integration that enables cost -effective electronic photonic integrated circuits (ePIC) [2]. On the other hand, testing ePICs at wafer level and module assembly come with challenges, leading to raised total costs for the DCI. Thus, packaging methods play an important role in determining the overall cost and performance of the electronic-photonic modules. In general, surface mount technology (SMT) assembly methods are used to improve automation. For instance, optical ball grid arrays (BGA) are used for increasing the frequency range (RF bandwidth) between DSP (Digital Signal Processing) and the optical module.

Revision and adaptation should be considered in the packaging of transceiver modules by using non-hermetic packages rather than traditional gold-box versions. Therefore, both the transceiver chip and the package should be SMT compatible, simpler in assembly similar to electronic ICs, and in line with the standardized processes [3] as illustrated in fig. 2.

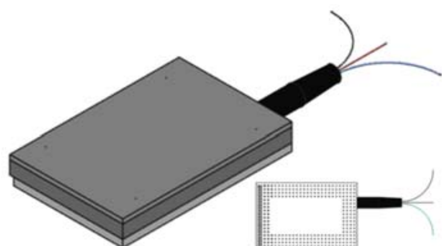

Fig. 1. IC-TROSA type-1 package (OIF)

References

[1] F. Boeuf *et al.*, *OFC*, W3A.1 (2015)
[2] D. Knoll *et al.*, *BCTM*, 88-96 (2015)
[3] Optical Internetworking Forum (OIF), *OIF-Tech-Options-400G-01.1* (2015)